Data Book
ZF 104Card™

PC/104 CPU Module
based on the
OEMmodule™

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General Description

The ZF 104Card represents the fastest way to incorporate a ZF MicroSystems' OEMmodule into a fully operational PC/104 system for hardware and software development. It is a complete PC/AT-compatible motherboard that can be used alone as an embedded controller or with other PC/104 modules in a complete system tailored to your needs. You can develop software on a desktop PC/AT and transfer your code directly to an OEMmodule-based embedded system with little or no modification, or you can develop your software directly on a ZF 104Card system.

The ZF 104Card includes all standard motherboard functions: serial and parallel I/O, floppy and EIDE disk controllers, an internal resident Flash disk for program storage, an optional True Flash File disk, PC/104 expansion bus, a standard PC/AT BIOS, and Embedded DOS™-ROM (EDOS-ROM)(386SX only).

For many systems, the standard PC ROM-BIOS and resident Flash disk with its EDOS-ROM (386SX) eliminate the need for rotating media (such as a floppy or hard disk) for application program storage.

INDUSTRY STANDARD PC/104 COMPATIBILITY

The ZF 104Card is compatible with the popular PC/104 standard, which allows you to easily integrate a wide variety of low-cost hardware peripherals in your embedded system.

The module's PC-compatible serial ports, parallel ports, floppy interface, and hard disk interface allow you to use standard hardware, cables, and software libraries in your development program.

Features

100 MHz 486SX or 40 MHz 386SX CPU

- Full 32-bit internal architecture, cost-effective 16-bit external bus.
- Virtual memory, paging, and hardware-enforced protection.
- Physical memory space of up to 18MB.

DRAM Controller

- High performance MUXed DRAM interleave, CPU pipelined operation.
- 2M DRAM on the OEMmodule.
- Supports additional 4M or 16M bytes SO-DIMM memory modules.
- Shadowed BIOS for optimum performance.

PC Core Logic

- AT-compatible DMA controllers, interrupt controllers, timer/counters .
- AT keyboard controller.
- Real-time clock.

Serial Ports

- Four independent PC-compatible 16550-compatible RS232C serial ports.

Parallel Ports

- Two fully-compatible PC/AT parallel ports.
- Bi-directional operation.

Floppy Disk Controller

- Supports all standard PC floppy formats.
- Software compatible with 765B floppy controller and PC BIOS.
- Integrated digital data separator for high reliability and noise immunity.

EIDE Hard Drive Interface

- Full 40-pin interface to standard EIDE hard disk drive.
- Supports up to two EIDE drives (master/slave).

Solid State M-System's True Flash™

- Uses "NAND" flash memory.
- Expandable by adding an external Flash memory device with capacities from 2MB (factory option).

Solid State Flash Storage

- 180 KB (386SX) or 1.4MB (486SX) Flash EPROM available for OS and OEM software.
- DOS-compatible BIOS in Flash EPROM.
- Can be configured to be the boot drive.
- Expandable up to 16MB additional on-board.

Expansion Bus

- Fully compliant with the PC/104 expansion bus.

Power Monitor

- Brownout protection; resistor-configurable voltage threshold.
- Provides reliable reset signal if power fluctuates.

PC BIOS

- Standard AT BIOS functionality.
- Easy to upgrade using ZF MicroSystem's unique Download Mode.
- Setup information is stored in non-volatile Flash EPROM. Allows battery-free operation.

Disk Operating System

- Caldera Software's Embedded DOS standard(386SX only).
- Supports most PC/AT-compatible operating systems, including MS-DOS.
- Supports Embedded DOS 6-XL, fully multi-threaded version compatible with standard DOS. Real-time designs benefit from true multi-threading from the kernel up. Embedded DOS features APIs for non-DOS file systems, and other optional features(386SX only).

Electrical Specifications

- 5 volt ±5% only operation — requires 5VDC @ 650mA (2 MB internal DRAM).
- Support for low-power modes (486SX only)

Mechanical/Environmental

- Compliant with PC/104 standard form factor.
- Standard PC/104 16-bit stackthrough connector for PC/104 modules.
- Standard ribbon cable connectors for floppy, EIDE, serial, and parallel interfaces.
- Operating temperature: 32F to 158F (0C to 70C).
- Storage temperature: -67F to 185F (-55C to 85C).
- Weight: 3.6 oz (102 gm).

ORDERING INFORMATION

104-386-Q-01/104-486-Q-01 — ZF 104Card, PC/104 module: OEMmodule, 4 serial, 2 parallel (the 2 serial and 1 parallel in the OEMmodule, plus 2 additional serial and one additional parallel). Bulk order. Does not include cables, manuals, additional Flash memory, or utility disk.

104-386-Q-02/104-486-Q-02 — ZF 104Card, PC/104 module: Same as Q-01, but with additional 2MB Flash EPROM.

104-386-Q-03/104-486-Q-03 — ZF 104Card, PC/104 module: Same as Q-01, but without additional 2 serial,/1 parallel.

104-386-Q-04/104-486-Q-04 — ZF 104Card, PC/104 module: Same as -Q-01, but with additional 2MB Flash EPROM and without additional 2 serial/1 parallel.

104-386-K-01/104-486-K-01 — ZF 104Card Development Kit: PC/104 module with OEMmodule 4 serial, 2 parallel (the 2 serial and 1 parallel in the OEMmodule, plus 2 additional serial and one additional parallel), additional 2 MB Flash EPROM, cables, utility software, and technical manual.

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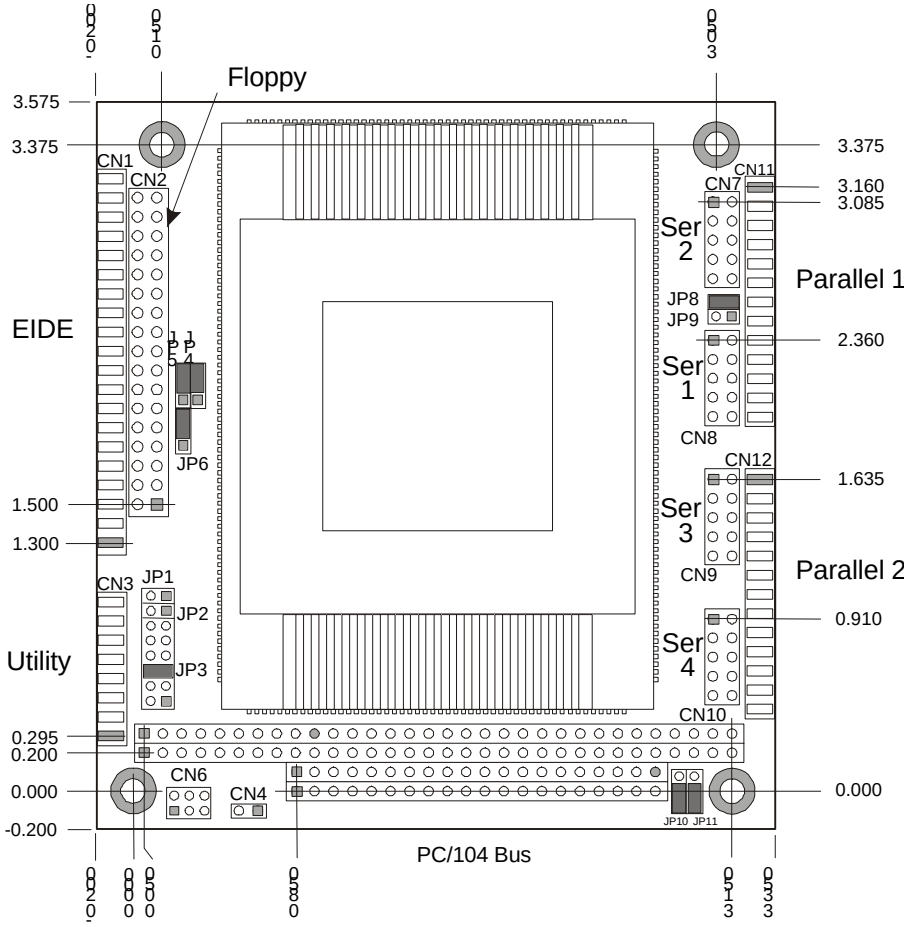

Figure 1. Board Dimensions

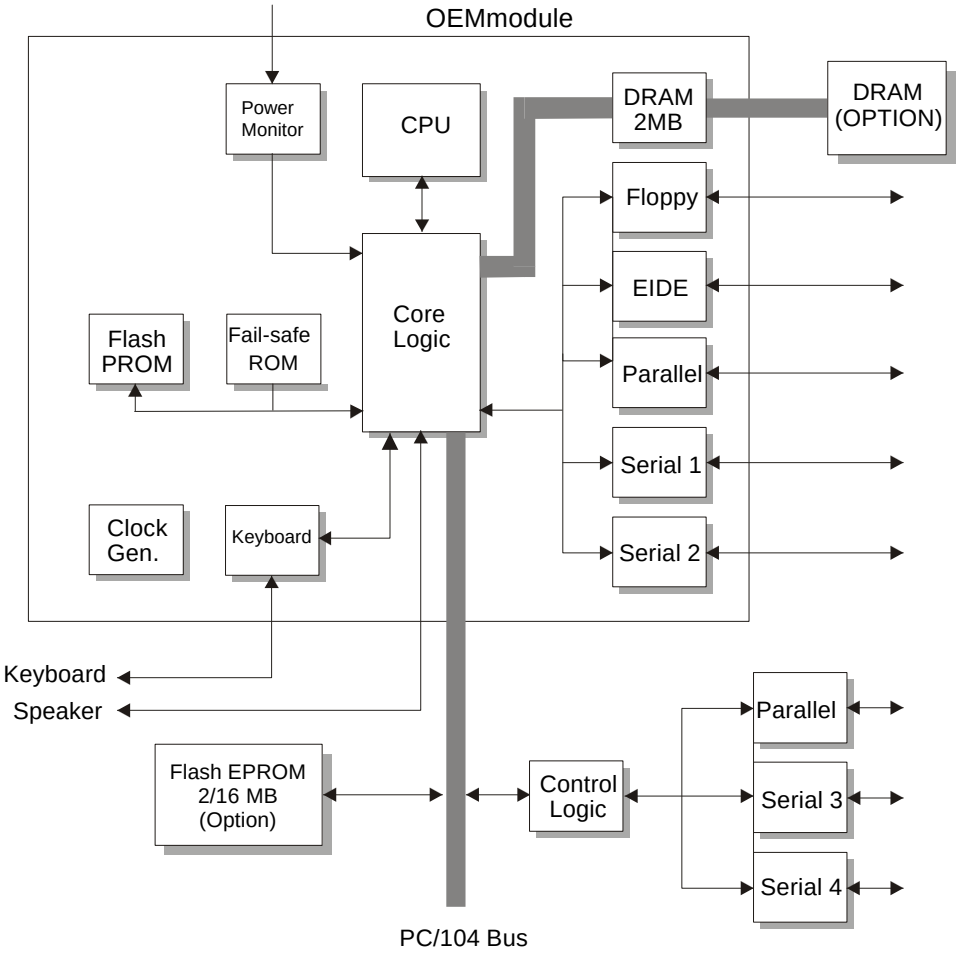

Figure 2. System Block Diagram

Jumper Summary

The ZF 104Card provides a number of jumper options to configure features on the board. The jumpers, labeled "JP*n*", are configured with 2mm shorting blocks. Table 1 shows a summary of the jumpers, their functions, and the factory default settings. For jumper options with more than two pins, default shorted pin-pairs are listed as *n1*/*n2*.

Jumper	Function	Default
JP1	BDIS- signal: On=Fail-Safe ROM, Off=Flash BIOS	Off
JP2	Not used	Off
JP3	True Flash File I/O address select: 1/2 (Reserved) 3/4 (Reserved) 5/6 D800h 7/8 D000h 9/10 C800h	5/6
JP4	Flash voltage select, 1/2 = 3.3V, 2/3 = 5V	2/3
JP5	DRAM voltage select, 1/2 = 3.3V, 2/3 = 5V	2/3
JP6	Flash controller voltage, 1/2 = 3.3V, 2/3 = 5V	2/3
JP8, JP9	JP8 JP9 Off Off No IRQ attached to LPT2 Off On IRQ7 attached to LPT2 On Off IRQ5 attached to LPT2 On On Not allowed	JP8 On JP9 Off
JP10, JP11	JP10 JP11 1/2 1/2 COM4 set to RS232C 2/3 2/3 Reserved	JP10 1/2 JP11 1/2
CN6	WDT Hardware Enable 1/2 Enabled On 386SX, M BIOS required.	Off

Table 1. Jumper Summary

Connector Summary

Most connections to the ZF 104Card are made through I/O connectors CN1 through CN12 and the PC/104 bus connectors P1 and P2. Table 2 summarizes the use of CN1 through CN12.

Connector	Function	Type
CN1	EIDE	40-Pin Dual Row, .100 centers
CN2	Floppy	34-Pin Dual Row, .100 centers
CN3	Utility	16-Pin Dual Row, .100 centers
CN4	(Reserved)	
CN5	Memory Expansion	72-Pin SO-DIMM (single-sided)
CN6	WDT (see table 1)	
CN7	Serial 2	10-Pin Dual Row, .100 centers
CN8	Serial 1	10-Pin Dual Row, .100 centers
CN9	Serial 3	10-Pin Dual Row, .100 centers
CN10	Serial 4	10-Pin Dual Row, .100 centers
CN11	Parallel 1	26-Pin Dual Row, .100 centers
CN12	Parallel 2	26-Pin Dual Row, .100 centers

Table 2. Connector Summary

DRAM Interface

The ZF 104Card is supplied with an SO-DIMM connector for standard 72-pin SO-DIMM modules. The interface is designed to support 70 nS or faster fast page-mode DRAMs.

SO-DIMM MODULES, 72-PIN FPM OR EDO(486SX ONLY)

Any standard page-mode SO-DIMMs ***non-doubled sided*** memory modules, 3.3V or 5V, with 70nS (or better) access time, can be used on boards equipped with the SO-DIMM socket (factory option). For 3.3V SO-DIMM operation, install a jumper block on JP5-1/2. For 5V operation install a jumper block on JP5-2/3.

SETTING MEMORY SIZE

The BIOS automatically senses the amount of memory installed in your system and displays that information on the Setup configuration page. There is no user setting.

Power and Utility Connector

Power to the board may be supplied through the 16-pin connector, CN3 or through the PC/104 bus. CN3 is recommended.

If you power the board through the PC/104 bus, refer to the PC/104 bus tables to determine which pins are used for power.

If you power the board through CN3, refer to Table 3 for pin assignments.

In addition to power, the keyboard, speaker, reset, and secondary power failure monitoring signals are provided on CN3.

PIN #	Description	PIN #	Description
1	Ground	2	Ground
3	+5 Volts	4	+5 Volts
5	VBat	6	-5 Volts
7	-12 Volts	8	+12 Volts
9	KClock	10	KData
11	Pwrdn-	12	MR-
13	PFI-	14	PFO-
15	Key Pin	16	Spkr-Out

Table 3. Power and Utility Connector

Note: CN3 is an edge-mounted PCB connector with odd number pins located on the module side of the board, and even number pins on the other side. Pin 1 of CN3 is located closest to the PC/104 bus connector J1. See Figure 1.

KEYBOARD

The ZF 104Card provides the standard keyboard signals, KClock and KData for connection to a standard PS/2 keyboard. Table 4 shows how to wire a DIN-5 connector for a standard PS/2 keyboard cable.

Signal Name	Pin	Function	5-Pin DIN
KClock	CN3-9	Keyboard Clock	1
KData	CN3-10	Keyboard Data	2
		N/C	3
Ground		Ground return	4
Power		Keyboard Power (+5 Volts)	5

Table 4. Keyboard Connector Wiring

SPEAKER

Small piezoelectric speakers or standard PC speakers (with an 8 ohm coil) can be directly driven by the ZF 104Card through connector CN3. To attach an external speaker, connect it to CN3-16 and CN3-3 (+5V). The port supplies approximately 0.1 watt to the speaker.

The ZF 104Card Utility Connector board, included with the ZF 104Card Development Kit, supplies a piezoelectric speaker and provides access to an external speaker via a screw terminal.

REAL-TIME CLOCK BATTERY

The real-time clock requires a 3.6 volt lithium cell to maintain the correct time, date, and CMOS memory values when power is off. Connect the battery to CN3-5 to CN3-1 (Ground)

If the battery is not present and power is removed, the RTC will lose the current time and date, but the Setup data will remain intact. CMOS configuration information is always read from a Flash EPROM copy (inside the OEMmodule) if there is a fault detected in the contents of the Setup parameters stored in the CMOS RAM portion of the RTC.

The ZF 104Card Utility Connector board, included with the ZF 104Card Development Kit, has two solder pads for a 1/2AA Lithium battery (Tadiran TL-5101/PBP, Panasonic BR1/2AE5SP), a standard 4-pin PC-style battery connector, and screw terminals for connecting an external battery or power supply.

POWER MONITORING CIRCUIT

There are two power up/power failure monitoring circuits:

1. When VCC goes below 4.60V, the main power monitoring circuit resets the board. The duration of the reset pulse is at least 200 ms (this is guaranteed when VCC is above 1V).
2. The second circuit monitors an external voltage at connector CN3-13. When the voltage at the CN3-13 drops below 1.25V, the PFO- signal CN3-14 is generated (active low) until the voltage returns above the threshold. If you do not plan to use this circuit, leave CN3-13 open.

WATCHDOG TIMER

A watchdog timer is a circuit designed to either reset, cause an interrupt, or initiate some other recovery action if your program or hardware does not indicate that it is running properly. It usually is implemented for processes or activities that have some time predictability, such as the length of time it takes to perform a particular software function or complete the movement (or other change) of some physical system.

A typical application, for example, would initialize the watchdog timer when certain software functions start and end, or when a limit switch or optical interrupter connected to one of the digital I/O pins changes state. If the software crashes or gets stuck in a loop, or if the mechanical switch is not closed, the watchdog timer times out, causing a system reset.

The 104Card has a built-in circuit that can generate a timeout after 1.6 seconds unless reset by its input signal, WDI. WDI is an internally-generated logic signal controlled by a BIOS call. As long as the timer is reset every 1.6 seconds or less, its output signal, WDO remains in its inactive state. Should the timer time out, the WDO signal goes high, triggering a reset. The watchdog timer is disabled on Power-up.

M-Systems Flash Disk

For technical information about the M-System Flash Disk, refer to the M-Systems' DOC2000 manual (supplied on diskette).

Use jumper JP3 to set the address for the True Flash File memory. The default is JP3-5/6, which sets the memory address to 0D800h. Table 1 shows the memory addresses you can select with JP3.

Serial Ports

The ZF 104Card provides four full-featured PC-compatible asynchronous RS232C serial ports. The serial ports are treated as COM1, COM2, COM3 and COM4 devices by DOS. Standard system resources are allocated to the serial ports, as shown in Table 5:

Serial Port	Connector	Typical Usage	I/O Address	Standard Interrupt
Serial 1	CN8	COM1	3F8h–3FFh	IRQ4 (shared)
Serial 2	CN7	COM2	2F8h–2FFh	IRQ3 (shared)
Serial 3	CN9	COM3	3E8h–3EFh	IRQ4 (shared)
Serial 4	CN10	COM4	2E8h–2EFh	IRQ3 (shared)

Table 5. Serial Port Resources

A full complement of input and output handshaking lines are implemented for all serial ports. Signals are at standard RS232C levels. The RS232C level converters provide the required voltage levels with internal +5 volt to ±9 volt converters, allowing for 5 Volt-only operation.

SERIAL PORT CONNECTORS

The serial ports are brought out to 10-pin dual-row ribbon-cable connectors CN7, CN8, CN9, and CN10. The connector pins are arranged to make it easy to construct a simple straight-through ribbon cable to a panel-mount DB-9 connector. Four cables with DB-9 connectors are provided with the ZF 104Card Cable Kit. Pinouts for the serial connectors are shown in Table 4.

DB-9 Pin	CN7, 8, 9 & 10	Signal	Function	In/Out
1	1	DCD	Data Carrier Detect	Input
2	3	RXD	Receive Data	Input
3	5	TXD	Transmit Data	Output
4	7	DTR	Data Terminal Ready	Output
5	9	GND	Signal Ground	
6	2	DSR	Data Set Ready	Input
7	4	RTS	Request To Send	Output
8	6	CTS	Clear To Send	Input
9	8	RI	Ring Indicator	Input
	10	N/C	No connection	

Table 6. Serial Port Connectors

Note: CN7, 8, 9 & 10 are right angle mounted PCB connector with odd number pins located on the module side of the board, and even number pins on the other side. Pin 1 of each connector is located farthest from the PC/104 bus connector J1.

SERIAL PORT INTERRUPT SHARING

The serial port interrupt request lines comply with the interrupt sharing scheme described in the PC/104 Version 2.3 specification. This sharing scheme is described in the OEMmodule Data Book.

The interrupt request lines from Serial 1 and Serial 2 are internally buffered in the OEMmodule with open collector buffers and internally connected to inputs IRQ4 and IRQ3 respectively. Internal 1000 ohm termination resistors hold the interrupt signals at logic 0 until an interrupt occurs. Other interrupt sources can be wire-ORed with either of these IRQ lines as long as they also follow the PC/104 interrupt sharing convention. The interrupt request signals appear on the PC/104 bus.

Note: The 1000 ohm pull-down resistor for each interrupt is provided in the module. Do not attach an external pull-down resistor.

Parallel Ports

The ZF 104Card parallel ports are fully compatible with the PC/AT parallel port. In the extended mode, they function as PS/2-like bi-directional ports. The parallel ports use the following PC resources:

Parallel Port	Connector	Typical Usage	I/O Address	Standard Interrupt
Parallel 1	CN11	LPT1	3BCh – 3BFh(386SX) 378h – 37Fh(486SX)	IRQ7
Parallel 2	CN12	LPT2	278h – 27Fh	IRQ5

Table 7. Parallel Port Resources

PARALLEL PORT INTERRUPT SHARING

The parallel port interrupts for LPT1 and LPT2 are both implemented with PC/104-type interrupt sharing logic.

LPT1 is assigned to IRQ7. LPT1 can share this interrupt with any other peripheral that also implements the PC/104 interrupt sharing scheme.

LPT2 can share IRQ7 with LPT1, or it can be jumpered to IRQ5. If it is connected to IRQ5, it can share this interrupt with any other peripheral that also implements the PC/104 interrupt sharing scheme.

Use JP8 and JP9 to configure parallel port interrupts, as shown in Table 8:

JP9	JP8	Result
Off	Off	No IRQ attached to LPT2
On	Off	IRQ7 attached to LPT2
Off	On	IRQ5 attached to LPT2
On	On	Not allowed

Table 8. Parallel Port Interrupts

Note: Do not install jumpers on both JP8 and JP9 at the same time.

Note: 1000 ohm pull-down resistors are provided on the ZF 104Card. Do not add additional pull-down resistors if you are sharing IRQ7 or IRQ5.

PARALLEL PORT SIGNALS

The parallel port output signals provide up to 48 mA drive current (active low). 2.2 nF capacitors are connected from each data line to ground for noise suppression.

PARALLEL PORT REGISTERS

Table 9 summarizes the parallel port register interface. In this table, “A” indicates the port’s base address, for example 378h.

Register	Bit	Signal Name	In/Out	Active High/Low
Data (A+0)	0	PD0	I/O	High
	1	PD1	I/O	High
	2	PD2	I/O	High
	3	PD3	I/O	High
	4	PD4	I/O	High
	5	PD5	I/O	High
	6	PD6	I/O	High
	7	PD7	I/O	High
Status (A+1))	0	1	-	-
	1	1	-	-
	2	1	-	-
	3	ERR-	In	Low
	4	SLCT-	In	High
	5	PE	In	High
	6	ACK-	In	High
	7	BUSY	In	Low
Control (A+2)	0	STRB-	Out	Low
	1	AUTOFD-	Out	Low
	2	INIT-	Out	High
	3	SLIN-	Out	Low
	4	IRQ ENABLE	-	High
	5	1	-	-
	6	1	-	-
	7		-	-

Table 9. Parallel Port Registers

The parallel port signals appear on CN11 and CN12, 26-pin dual-row ribbon-cable edge connectors. The port may be cabled to appear on standard PC DB-25 connectors. A DB-25 connector and cable are provided for this purpose in the ZF 104Card cable kit. Table 10 shows the parallel port signals appearing on CN11 and CN12 and the equivalent pinout on DB-25S connectors.

CN11 & CN12	DB-25S Pin	Signal	Function	In/Out
1	1	STRB-	Output Data Strobe	Output
2	14	AUTOFD-	Auto Feed	Output
3	2	PD0	Data Bit 0	I/O
4	15	ERR-	Printer Error	Input
5	3	PD1	Data Bit 1	I/O
6	16	INIT-	Initialize Printer	Output
7	4	PD2	Data Bit 2	I/O
8	17	SLIN-	Selects Printer	Output
9	5	PD3	Data Bit 3	I/O
10	18	GND	Signal Ground	N/A
11	6	PD4	Data Bit 4	I/O
12	19	GND	Signal Ground	N/A
13	7	PD5	Data Bit 5	I/O
14	20	GND	Signal Ground	N/A
15	8	PD6	Data Bit 6	I/O
16	21	GND	Signal Ground	N/A
17	9	PD7	Data Bit 7	I/O
18	22	GND	Signal Ground	N/A
19	10	ACK-	Character Acknowledged	Input
20	23	GND	Signal Ground	N/A
21	11	BUSY	Printer Busy	Input
22	24	GND	Signal Ground	N/A
23	12	PE	Out Of Paper	Input
24	25	GND	Signal Ground	N/A
25	13	SLCT	Printer Selected	Input
26	N/A	GND	Signal Ground	N/A

Table 10. Parallel Port Connectors

Note: CN11 and CN12 are edge mounted PCB connectors with odd number pins located on the module side of the board, and even number pins on the other side. Pin 1 of CN11 and CN12 are located farthest from the PC/104 bus connector J1.

Floppy Interface

A DOS-compatible floppy drive interface is supplied on CN2. This interface allows cable connection to two floppy drives. In PC-compatible systems, the BIOS and DOS support these drives as A: and B:. These are configured using the BIOS Setup function.

Table 11 shows the PC resources used by the floppy subsystem.

Resource	Function
I/O Address 3F0h-3F7h	3F2 FDC Digital Output Register (LDOR) 3F4 FDC Main Status Register 3F5 FDC Data Register 3F7 FDC Control Register (LDCR)
IRQ6	Interrupt
DRQ2–DACK2	DMA Controller Channel

Table 11. Floppy Interface Resources

The floppy drive interface supports the standard PC floppy disk formats, 360K, 1.2M, 720K, 1.44M, and 2.88M. You must specify the type of drives connected to the floppy interface in the BIOS CMOS Setup. Press <Del> during the Power-On Self Test (POST) to enter Setup. The first drive typically appears to DOS as drive A:, and the second drive as B:.

Floppy drives are normally connected to a system using ribbon cables. The typical PC connection for dual floppy drives uses a special cable with certain ribbon cable wires (conductors 10 through 16) reversed between the two floppy connectors. Using this arrangement, all floppy drives can be jumpered for drive select 1 (the “second” drive). The wires to drive B: are unswapped.

Note: The module’s internal Resident Flash Disk, if enabled, can be drive A or drive B . If the Flash disk is configured as drive A, any floppy disk drive configured as drive A will become Drive B automatically. Only two floppy drives (A and B) are supported.

Table 12 lists the signals on the CN2 floppy interface.

CN2 Pin	Signal Name	Function	In/Out
2	DENSEL	Speed/Precomp	
4	N/A		N/A
6	N/S	Key Pin	N/A
8	INDEX-	Index Pulse	In
10	MTR0-	Motor On 0	Out
12	DRV1-	Drive Select 2	Out
14	DRV0-	Drive Select 1	Out
16	MTR1-	Motor On 1	Out
18	DIR-	Direction Select	Out
20	STEP-	Step Pulse	Out
22	WDATA-	Write Data	Out
24	WGATE-	Write Gate	Out
26	TRK0-	Track 0	Input
28	WRPRT-	Write Protect	Input
30	RDATA-	Read Data	Input
32	HDSEL-	Head Select	Out
34	DSKCHG-	Disk Change	Input
1– 33 (Odd)	Ground	Ground	

Table 12. Floppy Drive Connector

Note: CN2 is a right angle mounted PCB connector with odd number pins located on the module side of the board, and even number pins on the other side. Pin 1 of the connector is located closest to the PC/104 bus connector J1.

EIDE Interface

The ZF 104Card is supplied with a standard EIDE Hard Disk Interface at connector CN1. This is the standard interface used in PC-compatible systems for hard disk drives. Up to two drives can be connected in a master-slave arrangement. Generally, the first hard disk drive (master) will appear as the C drive to DOS. The second drive, if attached, will appear as drive D. Table 13 lists the resources used by the EIDE interface.

Resource	Function
I/O Address 1F0h-1F7h	Hard Disk Interface
3F6h	Digital Output Register/Alternate Status Register
3F7h	Drive Address
IRQ14	Interrupt

Table 13. EIDE Interface Resources

Use Setup to enable your attached hard drives. You must match the drive parameters in Setup with the actual parameters of your connected drive(s).

EIDE drives are typically attached to the drive interface with a 40-pin ribbon cable. Miniature drives sometimes require a cable adapter circuit board for translation between the standard 0.1 inch-spacing connector and the smaller connector on the drive. These generally are supplied with the drive.

The pinout for the EIDE interface, CN1, is shown in Table 14.

Note: Due to drive manufacturer's different implementations of the master/slave arrangement, it may not be possible to properly configure drives from different sources to share the EIDE bus.

CN1 Pin	Signal Name	Function	In Out	CN1 Pin	Signal Name	Function	In Out
1	HDRESET-	Reset signal from host	OUT	21	N/A	Reserved	N/C
2	GND	Ground		22	GND	Ground	
3	HDD07	Data bit 7	I/O	23	HDIOW-	Write strobe	OUT
4	HDD08	Data bit 8	I/O	24	GND	Ground	
5	HDD06	Data bit 6	I/O	25	HDIOR-	Read strobe	OUT
6	HDD09	Data bit 9	I/O	26	GND	Ground	
7	HDD05	Data bit 5	I/O	27	RSVD	Reserved	N/C
8	HDD10	Data bit 10	I/O	28	HDALE	Address latch enable	OUT
9	HDD04	Data bit 4	I/O	29	RSVD	Reserved	N/C
10	HDD11	Data bit 11	I/O	30	GND	Ground	
11	HDD03	Data bit 3	I/O	31	IRQ14	Drive interrupt request	IN
12	HDD12	Data bit 12	I/O	32	IOCS16-	I/O Chip Select 16	In
13	HDD02	Data bit 2	I/O	33	HDA1	IDE Address 1	Out
14	HDD13	Data bit 13	I/O	34	RSVD	Reserved	N/C
15	HDD01	Data bit 1	I/O	35	HDA0	IDE Address 1	Out
16	HDD14	Data bit 14	I/O	36	HDA2	IDE Address 2	Out
17	HDD00	Data bit 0	I/O	37	HDCS0-	IDE Chip Select 0	Out
18	HDD15	Data bit 15	I/O	38	HDCS1-	IDE Chip Select 1	Out
19	GND	Ground		39	LEDIN-		
20	KEY	Keyed pin	N/C	40	GND	Ground	

Table 14. EIDE Drive Connector

Note: CN1 is an edge mounted PCB connector with odd number pins located on the module side of the board, and even number pins on the other side. Pin 1 of CN1 is located closest to the PC/104 bus connector J1.

Note: For maximum reliability, limit EIDE drive cables to less than 18 inches long.

PC/104 Expansion Bus Interface

Table 15 through Table 18 document the PC/104 expansion bus provided on the ZF 104Card module. It also includes the pin designations for the standard ISA expansion bus interface signals for reference to standard PC bus expansion cards.

PC/104 P1A	ISA	Signal Name	Function	In/out
A1	A1	IOCHCK-	Bus NMI input	In
A2	A2	SD7	System Data bit 7	I/O
A3	A3	SD6	System Data bit 6	I/O
A4	A4	SD5	System Data bit 5	I/O
A5	A5	SD4	System Data bit 4	I/O
A6	A6	SD3	System Data bit 3	I/O
A7	A7	SD2	System Data bit 2	I/O
A8	A8	SD1	System Data bit 1	I/O
A9	A9	SD0	System Data bit 0	I/O
A10	A10	IOCHRDY	Processor Ready Ctrl	In
A11	A11	AEN	Address Enable	I/O
A12	A12	SA19	Address bit 19	I/O
A13	A13	SA18	Address bit 18	I/O
A14	A14	SA17	Address bit 17	I/O
A15	A15	SA16	Address bit 16	I/O
A16	A16	SA15	Address bit 15	I/O
A17	A17	SA14	Address bit 14	I/O
A18	A18	SA13	Address bit 13	I/O
A19	A19	SA12	Address bit 12	I/O
A20	A20	SA11	Address bit 11	I/O
A21	A21	SA10	Address bit 10	I/O
A22	A22	SA9	Address bit 9	I/O
A23	A23	SA8	Address bit 8	I/O
A24	A24	SA7	Address bit 7	I/O
A25	A25	SA6	Address bit 6	I/O
A26	A26	SA5	Address bit 5	I/O
A27	A27	SA4	Address bit 4	I/O
A28	A28	SA3	Address bit 3	I/O
A29	A29	SA2	Address bit 2	I/O
A30	A30	SA1	Address bit 1	I/O
A31	A31	SA0	Address bit 0	I/O
A32		GND	Ground	N/A

Table 15. PC/104 Expansion Bus Connector, A1 -A32

PC/104 P1B	ISA	Signal Name	Function	In/out
B1	B1	GND	Ground	N/A
B2	B2	RESETDRV	System reset signal	Out
B3	B3	+5V	+5 volt power	N/A
B4	B4	IRQ9	Interrupt request 9	In
B5	B5	-5V		N/A
B6	B6	DRQ2	DMA request 2	In
B7	B7	-12V		N/A
B8	B8	ENDXFR- (0WS-)	Zero wait state (note 1)	In
B9	B9	+12V		N/A
B10	B10			
B11	B11	SMEMW-	Mem Write (lower 1MB)	I/O
B12	B12	SMEMR-	Mem Read (lower 1MB)	I/O
B13	B13	IOW-	I/O Write	I/O
B14	B14	IOR-	I/O Read	I/O
B15	B15	DACK3-	DMA Acknowledge 3 (note 1)	Out
B16	B16	DRQ3	DMA Request 3 (note 1)	In
B17	B17	DACK1-	DMA Acknowledge 1	Out
B18	B18	DRQ1	DMA Request 1	In
B19	B19	REFRESH-	Memory Refresh (note 1)	I/O
B20	B20	SYSCLK	System clock (8 MHz)	Out
B21	B21	IRQ7	Interrupt Request 7	In
B22	B22	IRQ6	Interrupt Request 6	In
B23	B23	IRQ5	Interrupt Request 5	In
B24	B24	IRQ4	Interrupt Request 4	In
B25	B25	IRQ3	Interrupt Request 3	In
B26	B26	DACK2-	DMA Acknowledge 2	Out
B27	B27	TC	DMA Terminal Count	Out
B28	B28	BALE	Address latch enable	Out
B29	B29	+5V	+5 volt power	N/A
B30	B30	OSC	14.318 MHz clock	Out
B31	B31	GND	Ground	N/A
B32		GND	Ground	N/A

Note 1: These signals are not supported on the 486SX version.

Table 16. PC/104 Expansion Bus Connector, B1 -B32

PC/104 P2C	ISA	Signal name	Function	In/out
C0		GND	Ground	N/A
C1	C1	SBHE-	Bus High Enable	I/O
C2	C2	LA23	Address bit 23	I/O
C3	C3	LA22	Address bit 22	I/O
C4	C4	LA21	Address bit 21	I/O
C5	C5	LA20	Address bit 20	I/O
C6	C6	LA19	Address bit 19	I/O
C7	C7	LA18	Address bit 18	I/O
C8	C8	LA17	Address bit 17	I/O
C9	C9	MEMR-	Memory Read	I/O
C10	C10	MEMW-	Memory Write	I/O
C11	C11	SD8	System Data bit 8	I/O
C12	C12	SD9	System Data bit 9	I/O
C13	C13	SD10	System Data bit 10	I/O
C14	C14	SD11	System Data bit 11	I/O
C15	C15	SD12	System Data bit 12	I/O

PC/104 P2D	ISA	Signal Name	Function	In/out
D0		GND	Ground	N/A
D1	D1	MEMCS16-	16-bit memory access	In
D2	D2	IOCS16-	16-bit I/O access	In
D3	D3	IRQ10	Interrupt Request 10 (note 1)	In
D4	D4	IRQ11	Interrupt Request 11 (note 1)	In
D5	D5	IRQ12	Interrupt Request 12 (note 1)	In
D6	D6	IRQ15	Interrupt Request 15 (note 1)	In
D7	D7	IRQ14	Interrupt Request 14	In
D8	D8	DACK0-	DMA Acknowledge 0 (note 1)	Out
D9	D9	DRQ0	DMA Request 0 (note 1)	In
D10	D10	DACK5-	DMA Acknowledge 5 (note 1)	Out
D11	D11	DRQ5	DMA Request 5 (note 1)	In
D12	D12	DACK6-	DMA Acknowledge 6 (note 1)	Out
D13	D13	DRQ6	DMA Request 6 (note 1)	In
D14	D14	DACK7-	DMA Acknowledge 7 (note 1)	Out
D15	D15	DRQ7	DMA Request 7 (note 1)	In
D16	D16	+5V	+5 volt power	N/A
D17	D17	MASTER-	Bus master assert (note 1)	In
D18	D18	GND	Ground	N/A
D19		GND	Ground	N/A

Note 1: These signals are not supported on the 486SX version.

Table 18. PC/104 Expansion Bus Connector, D0 -D19

BIOS Setup

The ZF 104Card system BIOS (Basic Input Output System) supports a standard Setup function to configure system parameters (as well as advanced methods specifically designed for embedded systems — refer to the OEMmodule Data Book for details). The BIOS uses the Setup parameters to establish default conditions during system initialization, both during the Power On Self Test (POST) phase, and during system boot.

Setup parameters are normally stored in the CMOS configuration memory, a portion of the real-time-clock circuit. In the OEMmodule, the configuration data is also stored in an internal Flash memory device. Therefore, if there is no clock battery present in the system, or if the battery fails, configuration data is not lost when power is turned off. The BIOS automatically loads configuration values from the Flash copy of the data.

Note: If you do not use a battery in your system, leave the battery input open.

USING SETUP

To enter the Setup function, press the <Del> key during POST. There will be a message displayed on the screen when <DEL> can be used.

Note: When you change Setup parameters, the new values do not take effect until the system is rebooted.

The Setup screens are as follows:

- **Main Menu Screen** — Displays a top-level menu of Setup choices
- **Basic CMOS Configuration** — Displays the standard CMOS options you can set for your system. For details about how to set the various parameters using Setup, refer to the OEMmodule Data Book.
- **Custom Configuration(486SX only)** — Displays the custom CMOS options available on the 486SX.

In addition to the various Custom Configuration parameters shown in the OEMmodule 486 Data Book, the following parameters are available only on the 104Card 486:

- **LPT2** — LPT2 can be set to Standard (AT), Bi-Dir (PS/2), EPP, or Disabled. The IRQ for LPT2 can be set to IRQ5 or IRQ7(jumper selectable) or Disabled.
- **COM3,COM4** — the following parameters can be set:
  - COM3 Enabled/Disabled
  - COM4 Enabled/Disabled
  - COM3 IRQ Disabled/IRQ3/IRQ4
  - COM4 IRQ Disabled/IRQ3/IRQ4

Embedded DOS-ROM (386SX only)

Each ZF 104Card has Caldera's Embedded DOS-ROM installed in Flash memory internal to the OEMmodule. The system can be set up to boot directly from DOS-ROM.

Full documentation of the many features and functions of DOS-ROM is beyond the scope of this manual. Full documentation is provided in a separate manual.

Specifications

ABSOLUTE MAXIMUM RATINGS*

Absolute Maximum Voltage on any pin, with respect to Ground ..... -0.3V to +6.5V

Storage Temperature (case) .....-55°C to +80°C (-67°F to +176°F)

OPERATING CONDITIONS*

Supply Voltage (V_{CC}) .....4.75V to +5.25V

Case Temperature (under bias) .....0°C to 70°C (32°F to 158°F)

* Stresses above those listed above can cause permanent damage to the board. These values are stress ratings only and do not imply that the device should be operated at these extremes. Exposure beyond the "Operating Conditions" may affect device reliability.

Note that some power supplies exhibit voltage spikes when AC power is switched on or off or when voltage transients appear on the AC power line. If this possibility exists, use a clamp circuit on the DC supply.

Literature References

The following references are for information about the PC architecture, the 386SX microprocessor, the PC DOS, and the PC BIOS.

ISA System Architecture

MindShare, Inc., Tom Shanley and Don Anderson
Internet: mindshar@interserv.com
CompuServe: 72507,1054
Published by Addison Wesley, Inc.
http://www.mindshare.com/

AT Bus Design

Edward Solari
Anabooks
12145 Alta Carmel Ct., Suite 250
San Diego, CA 92128
http://www.annabooks.com/

Personal Computer Bus Standard P996

Institute of Electrical and Electronic Engineers, Inc.
445 Hoes Lane
Piscataway, NJ 08854
http://www.ieee.org

MS-DOS References

MS-DOS Functions, Ray Duncan, Microsoft Press

MS-DOS Programmer's Reference, Microsoft Press, Microsoft Corporation

Undocumented DOS, Andrew Schulmen, Addison/Wesley

Technical data on the 386/486 SX microprocessor:

Intel
1751 Fox Drive
Suite 29000
San Jose, CA 95131
http://www.intel.com/

Technical data on Embedded DOS 6-XL

General Software, Incorporated
P.O. Box 2571
Redmond, WA 98073
Phone: (206)454-5755
FAX: (206) 454-5744
Email: general@gensoft.wa.com
BBS: (206) 454-5894

Technical data on Maxim RS232C buffers:

Maxim Integrated Products, Inc.
510 N. Pastoria Avenue
Sunnyvale, CA 94086
Htpp://www.questlink.com/index/maixm.html

The LIM 4.0 Expanded Memory Specification:

Lotus/Intel/Microsoft Expanded Memory Specification, Version 4.0
Lotus Development Corporation
55 Cambridge Parkway
Cambridge, MA 02142

PC/104 Consortium

809 B-175 Cuesta Drive,
Mountain View, CA 94040
Phone: 415 903-8304
FAX: 415 967-0995

MANUAL REVISIONS

Page	Revision	Date
All	Revision a	2/9/98
All	Revision b	7/98
All	Revision c	2/22/99

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